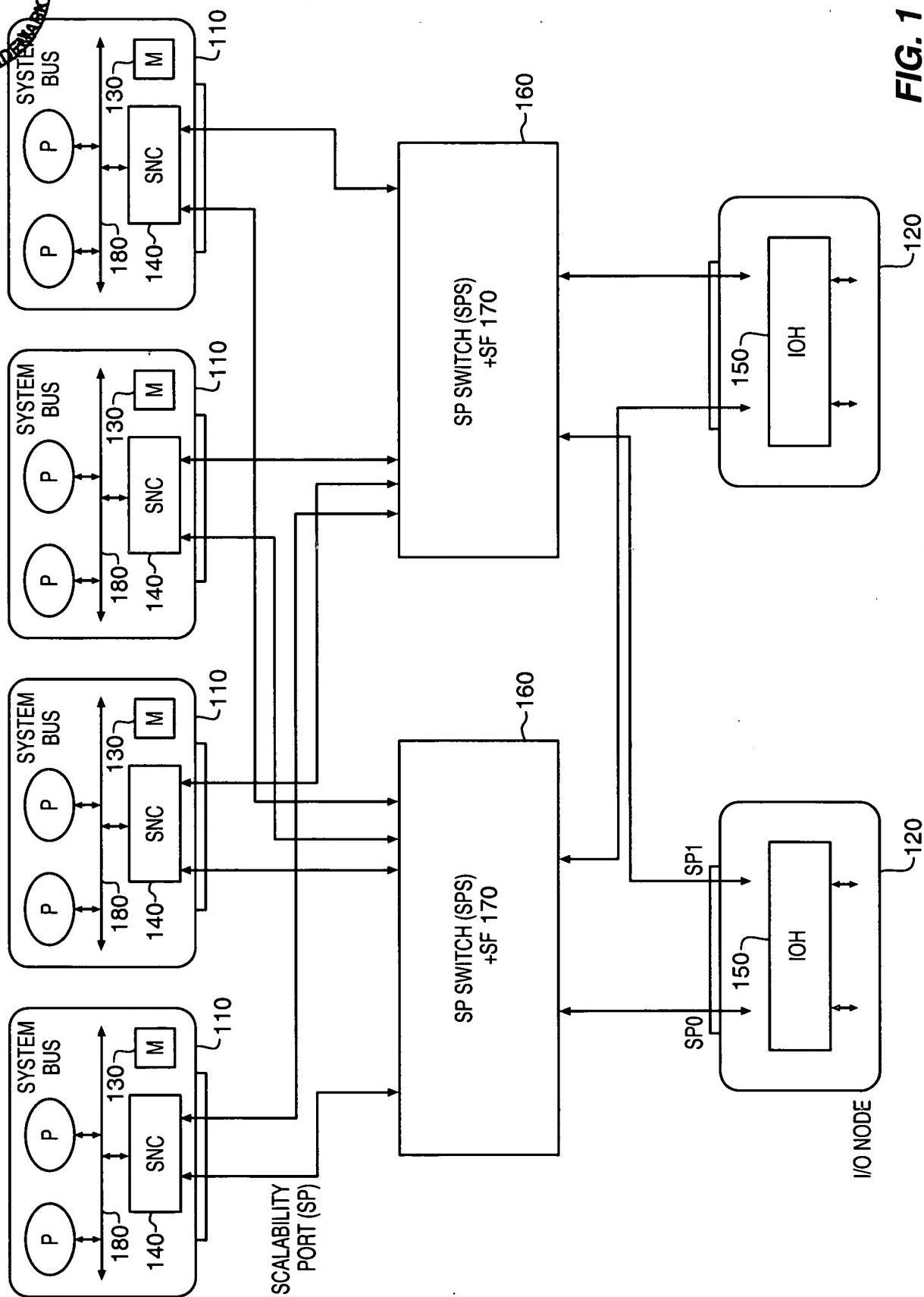
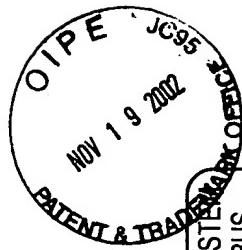


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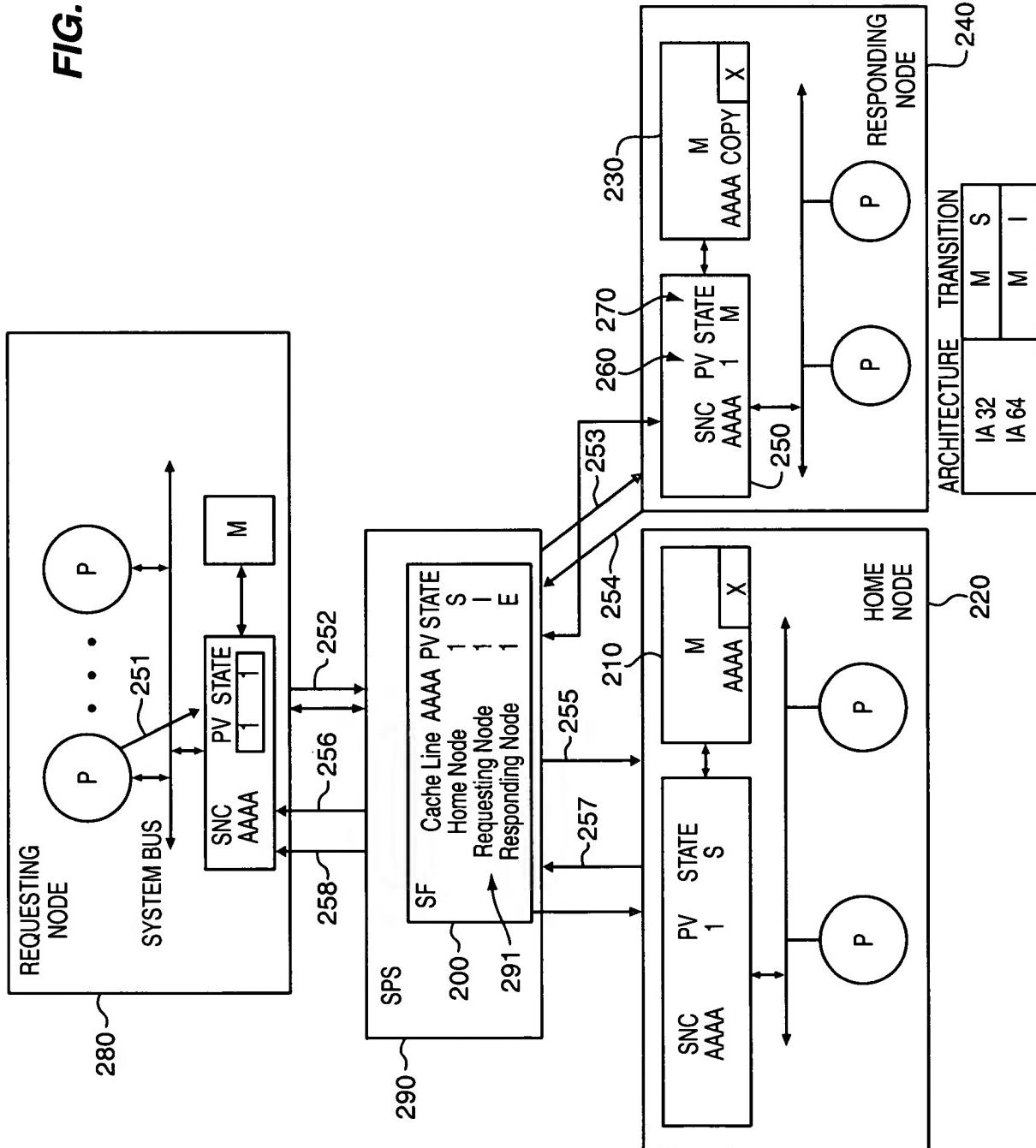




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A Mechanism for Efficiently Supporting the Full MIS (Modified, Invalid, Shared, Invalid) Protocol in a Cache Coherent Multi-Processor Shared Memory System
Inventor: Manoj Khare, et al.
Filing Date: December 29, 2000
Serial No.: 09/752,534
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FIG. 2



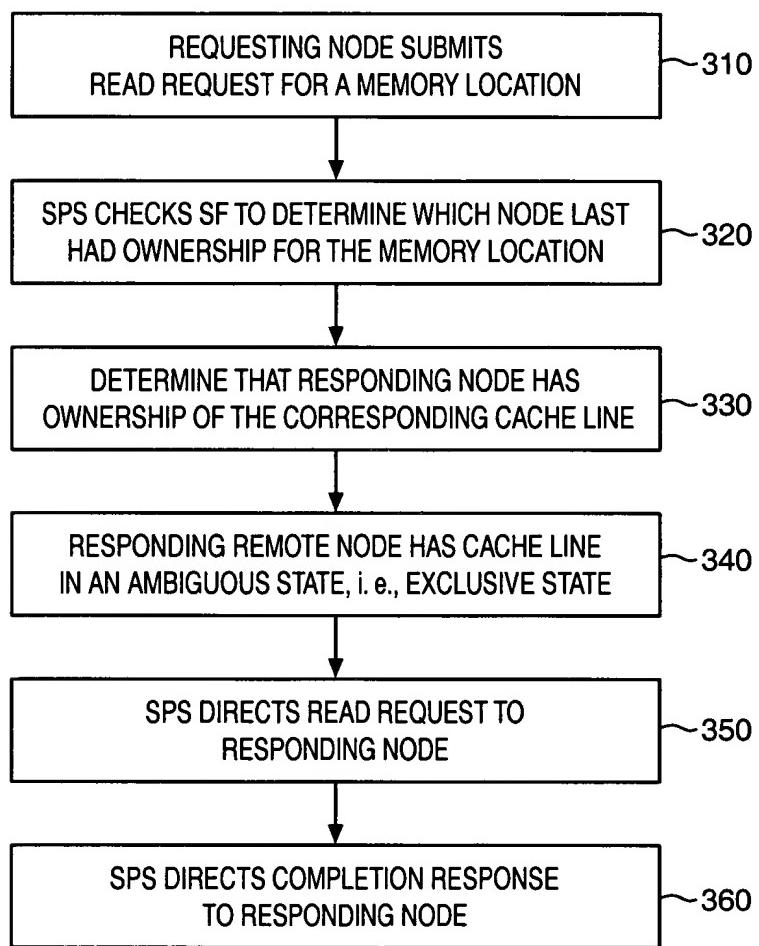
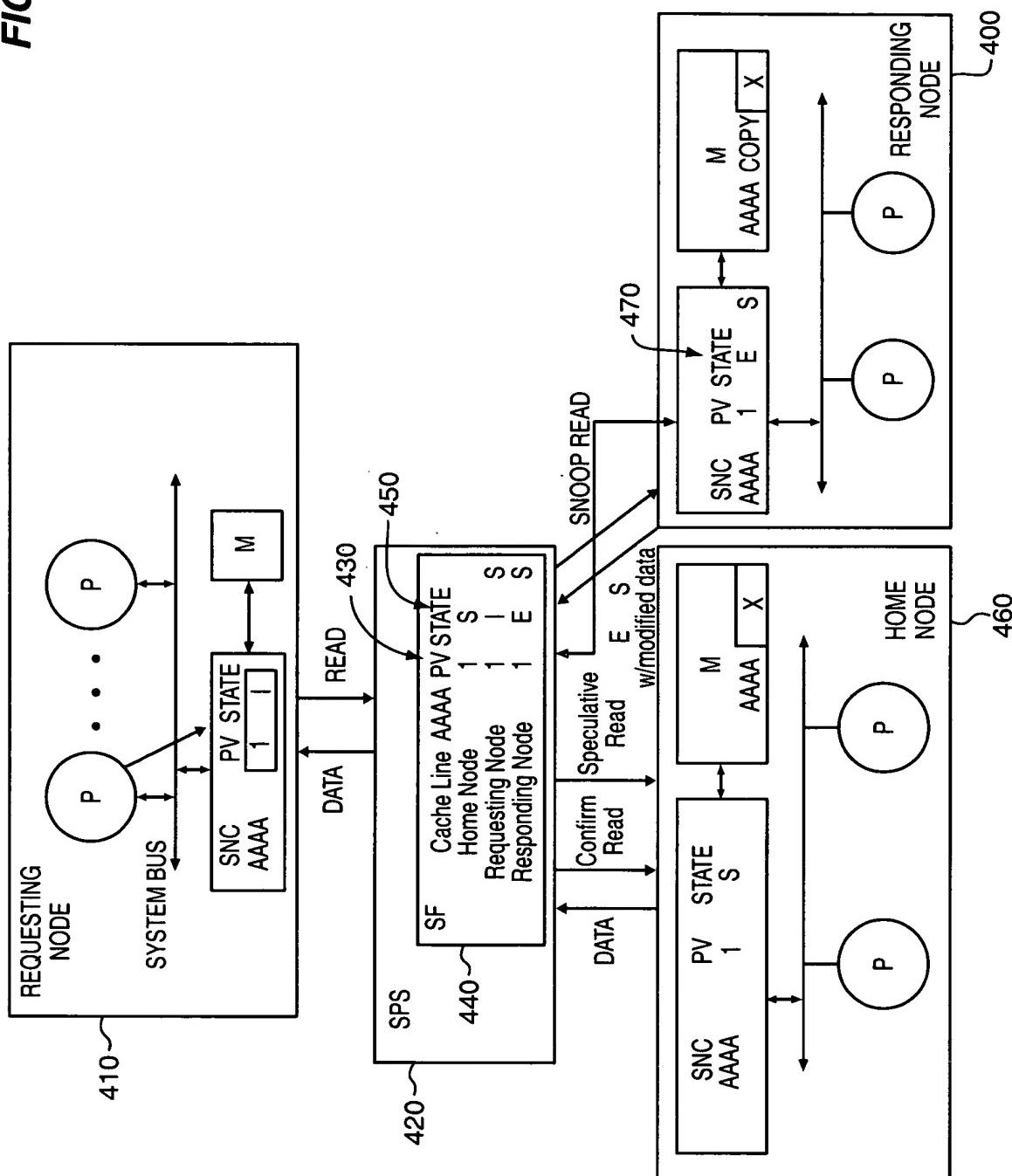
**FIG. 3**



FIG. 4



Shared Memory System

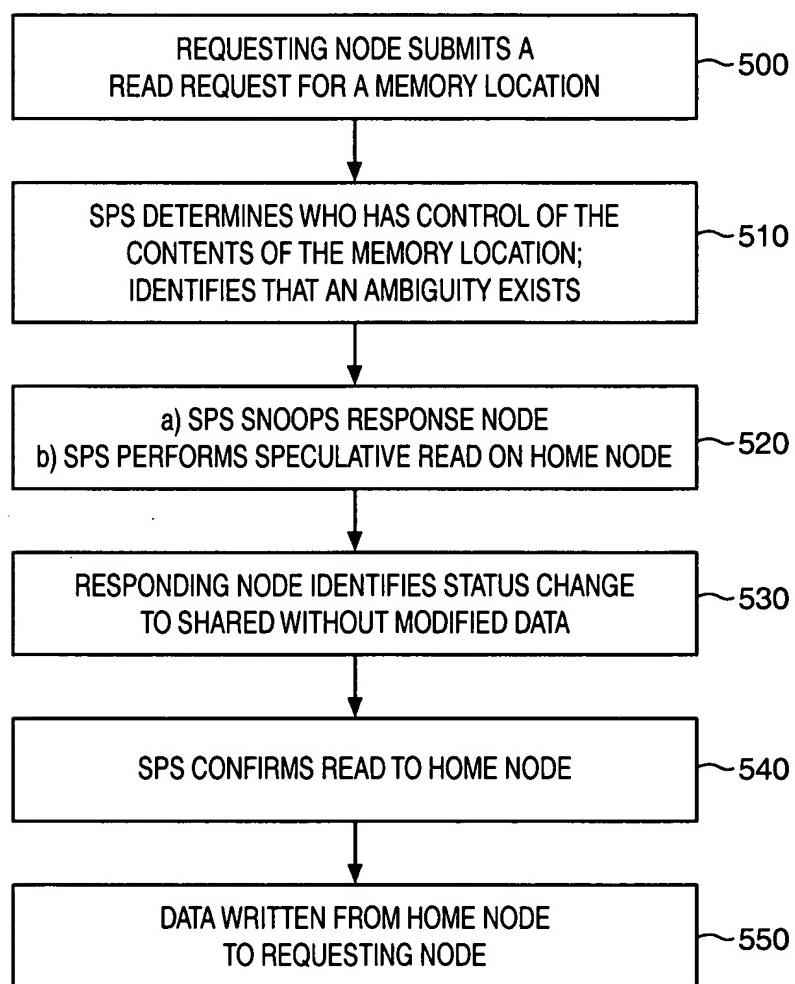
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**FIG. 5**

Title: A Mechanism for Efficiently Supporting Null Memory Modified, Exclusive, Shared, Invalid) Protocol in a Multi-Node Shared Memory System

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FIG. 6

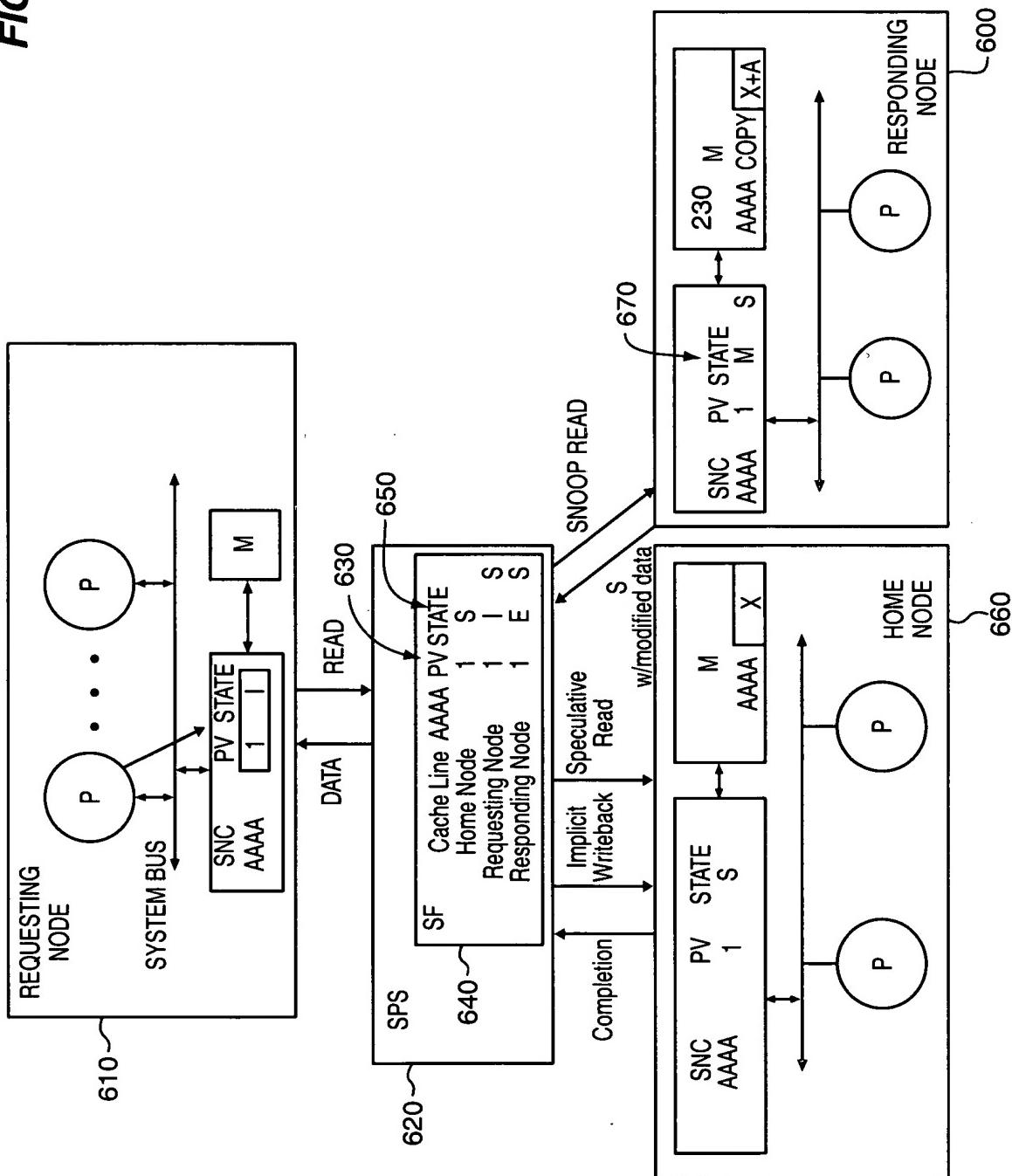
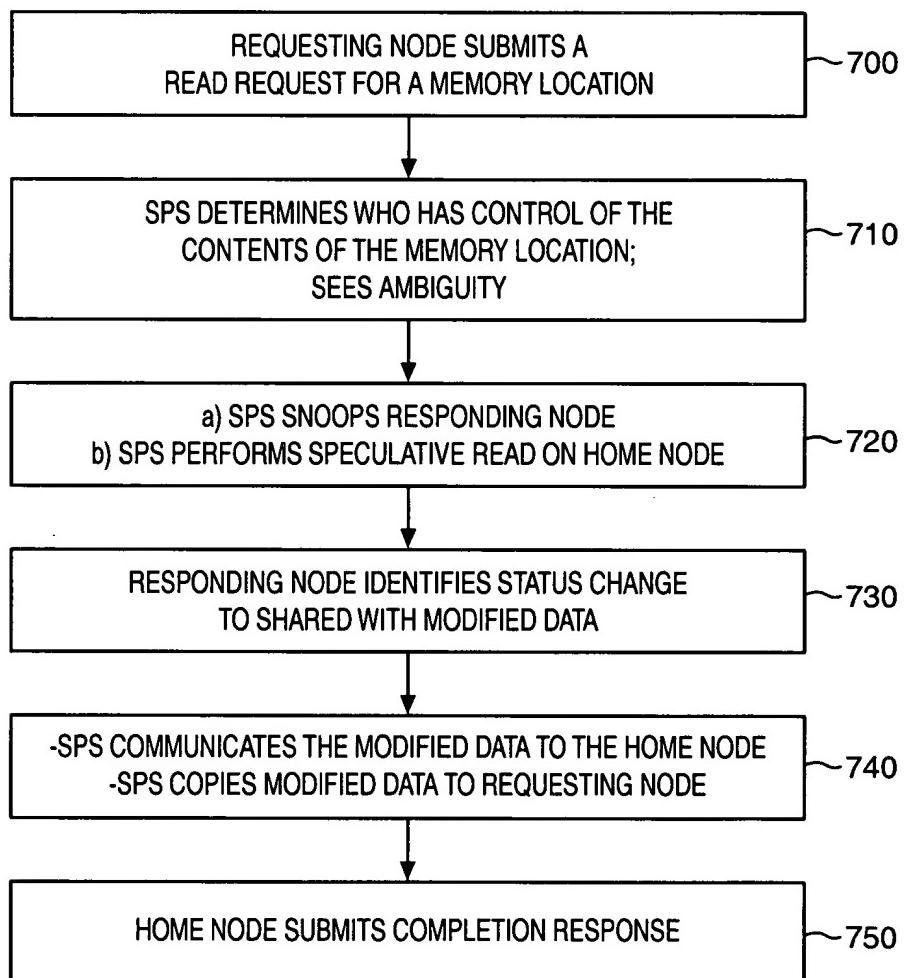




FIG. 7



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Shared Memory System
Inventor: Manoj Khare, et al.
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(303) 740-1980

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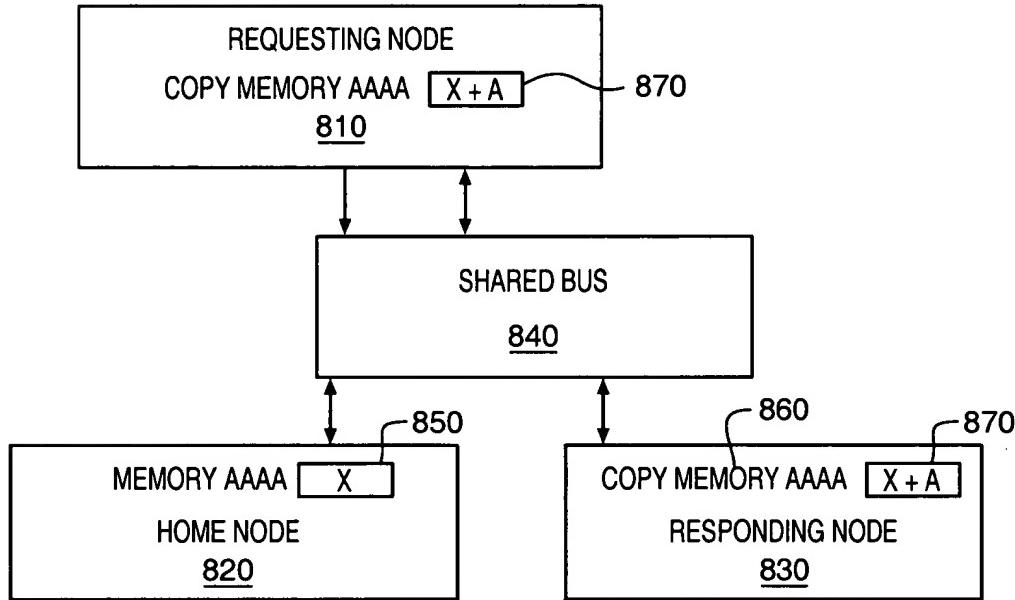


FIG. 8
PRIOR ART



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Title: A Mechanism for Efficiently Supporting the MES (Modified,
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Inventor: Manoj Khar, et al.
Filing Date: December 29, 2000
Serial No.: 09/752,534
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FIG. 9
PRIOR ART

